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AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): Hwa Sung RHEE et al.				Docket No. SEC.891D	
Application No. 10/619,581	Filing Date July 16, 2003	Examiner Walter Lee Lindsay, Jr.	Customer No. 20987	Group Art Unit 2812	Confirmation No. 7431

Invention: **SEMICONDUCTOR DEVICE HAVING HETERO GRAIN STACK GATE AND METHOD OF FORMING THE SAME**

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Transmitted herewith is an amendment in the above-identified application.

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CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
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Dated: **NOVEMBER 16, 2004**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent application of :

Hwa Sung RHEE et al. : Group Art Unit: 2812

Application Serial No.: 10/619,581 : Examiner: LINDSAY, Walter Lee, Jr.

Filed: July 16, 2003 :

SEMICONDUCTOR DEVICE HAVING HETERO GRAIN STACK GATE AND METHOD OF FORMING THE SAME

Request for Reconsideration and Correction of Drawings

U.S. Patent and Trademark Office
220 20th Street S.
Customer Window, Mail Stop **Amendment**
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Sir:

In response to the Office Action dated August 23, 2004, the drawings have been amended to correct a typographical error as shown in the attached amended drawings. In addition, a request for reconsideration of claims rejected by the Office Action is made herein.

In the Office Action, claims 13 and 18-21 were rejected under 35 U.S.C. §103 as being unpatentable over Murthy et al. (U.S. Patent No. 6,373,112) in view of Wu (U.S. Patent No. 5,773,348). Claims 14-16 were rejected under 35 U.S.C. §103 as being unpatentable over Murthy et al. in view of Wu as applied to claim 13, and further in view of Schinella (U.S. Patent No. 6,730,588). Claim 17 was

rejected under 35 U.S.C. §103 as being unpatentable over Murthy et al. in view of Wu as applied to claim 13, and further in view of Yu (U.S. Patent No. 6,743,680). Applicants respectfully traverse these rejections and request reconsideration of claims 13-21.

In rejecting independent claim 13, the Office Action describes Murthy as showing the following portions of the claimed method: "depositing a gate insulating layer (104), over a surface of a semiconductor substrate (102) (col. 4, lines 7-19), and depositing a lower poly-SiGe layer (112) having a columnar crystalline structure over the gate insulating layer... (col. 4, lines 7-19)." (See, Office Action at page 3, lines 1-5). The Office Action states that in contrast to the present invention, "Murthy shows that a poly-SiGe layer is used as a lower gate electrode and is set under an upper poly-Si gate electrode (col. 5, lines 10-21)." (See, Office Action at page 3, lines 16-17).

Indeed, the method suggested in the Office Action in relation to Murthy is very similar to the background in the subject application. See, for example, the conventional gate structure formed by the method illustrated in FIG. 2 of the subject application. Thus, features ascribed to Murthy by the Office Action reference add nothing to the present patentability discussion.

To remediate the noted deficiencies in Murthy, the Office Action cites Wu as a secondary reference in the rejection of claim 13. The Office Action alleges

that Wu teaches a method related to the formation of "a similar device." (See, Office Action at page 3, lines 18-19). Applicants respectfully disagree. Whereas the present invention claims in combination "a gate electrode includ[ing] a lower poly-SiGe layer having a columnar crystalline structure, and an upper poly-Si layer having a random crystalline structure", Wu fails to mention any layer or component formed from Germanium. This failure is non-trivial as described, for example, on page 5, paragraphs 0085, 0090, and 0095 of the subject specification. Absent a poly-SiGe layer, Wu does not describe or in any way relate to a "similar device."

The Office Action continues by stating that Wu teaches "a method of using an amorphous silicon gate that is annealed to form a polysilicon gate." Polysilicon is often formed by annealing an amorphous silicon layer. In fact, a number of methodologies exist for annealing amorphous silicon to form polysilicon. Depending on the conditions under which amorphous silicon is annealed, polysilicon may take on one of several different crystalline forms (i.e., possess various grain characteristics). For example, the structure of polysilicon may contain "domains with large-angle grain boundaries, twin boundaries, or both." See, Murthy et al., at col. 2, lines 54-55. Besides temperature, one variable affecting the crystallization of amorphous silicon is the presence or absence of an underlying poly-SiGe layer. As explained in relation to one exemplary

embodiment of the present invention, the composition of a lower layer may influence the crystalline form of an upper layer, "when the temperature is more than 500°C., crystallization starts at an interface region in contact with the lower poly-SiGe layer during the amorphous Si deposition process, wherein the amorphous Si layer has a continuous columnar structure as shown in FIG. 5." (See, pages 10-11, paragraph 0225 of the subject application). Therefore, because Wu is materially unrelated to the device and method claimed in the subject application, its combination with Murthy et al., or any similar disclosure, omitting a poly-SiGe layer, is unwarranted.

Additionally, Wu fails to teach any particular form of crystallization. Claim 13 recites in combination a method comprising, "crystallizing the amorphous Si layer to obtain an upper poly-Si layer having a *random crystalline structure.*" (Emphasis added). Wu certainly does not directly disclose any relationship between an annealing process as applied to an amorphous silicon layer in order to obtain a polysilicon layer having a *random crystalline structure*. Any conclusion to the contrary is pure speculation on the part of the Office. Because Wu fails to disclose a polysilicon layer having a random crystalline structure, a combination of Wu and Murthy et al. cannot reasonably be said to render obvious the invention of claim 13.

Most importantly and contrary to the dictates of 35 U.S.C. § 103, the prior art contains no motivation to combine Murthy et al. and Wu. The Office Action airily asserts that "Wu uses these fabrication methods in order to prevent the substrate from being damaged" and then leaps to the conclusion that "[i]t would have been obvious...to modify the method of Murthy...by replacing the polysilicon deposition process used un Murthy, with the motivation that the annealing of the amorphous silicon will cause less damage to the substrate." (See, Office Action, p. 4, lines 1-5). This supposed motivation to combine Wu with Murthy et al. is utterly misplaced for a number of reasons. First, Wu's concern for damaging the substrate has to do with the fact that "when removing [a] thick mask oxide, there is no protection for the underlying substrate." (See, Wu, at col. 1, lines 57-58). In the Wu method, a "pad nitride layer...serves as an etching stop layer during the step of removing the LPD oxide layer" (See, Wu at col. 2, lines 55-57). Since Murthy et al. does not disclose a step of removing a corresponding oxide layer, there is no possible aspect of Murthy et al. wherein combining it with Wu facilitates "less damage to the substrate." Finally, whereas Wu recites a single poly-Si layer separated from the substrate by pad oxide/nitride layers, Murthy et al. recite a poly-Si layer having a lower poly-SiGe layer interposed between itself and the substrate. Referring to FIG. 5 of Murthy et al., poly-SiGe layer 112 is interposed between upper poly-Si layer 110 and the substrate. Due to the presence

of interposed layer 112, substrate 102, including the gate oxide layer so jealously guarded by Wu, couldn't possibly be damaged by processing steps related to the formation of layer 110 in Murthy et al. As a result, the postulated combination of Wu with Murthy et al. could not possibly accomplish the purpose of "caus[ing] less damage to the substrate," and therefore the supposed motivation to combine Wu and Murthy et al. fails.

In summary, the combination of Murthy et al. and Wu is not proper under 35 U.S.C. § 103. First, Wu is materially unrelated to the device and method claimed in the subject application, and therefore its combination with Murthy et al. or any similar disclosure, omitting a poly-SiGe layer, is unwarranted. Next, Wu fails to disclose a polysilicon layer having a random crystalline structure, and hence the proposed combination of Wu and Murthy et al. does not obviate the invention of claim 13. Finally, no legitimate motivation to combine Murthy et al. and Wu exists in the prior art taken as a whole and Wu in particular. The motivation to combine Wu with Murthy et al. postulated by the Office Action is severely misplaced in relation to a supposed benefits provided by Wu that could not possibly apply to the method and device disclosed in Murthy et al.

For *at least* the reasons stated above, applicants respectfully contend that independent claim 13 would not have been obvious to one of ordinary skill in art in view of the combination of documents presented in the Office Action.

Accordingly, applicants request allowance of independent claim 13. Claims 14-21 depend from claim 13 and should likewise be allowed based on at least the distinctions made above in relation to claim 13.

Conclusion

No other issues remaining, reconsideration and favorable action upon claims 13-21 are requested.

Respectfully submitted,

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